A Technology Mapping Algorithm for MTJ-based LUT

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Field Programmable Gate Array(FPGA)s are composed of numerous SRAM-based lookup tables(LUTs). However, due to malicious characteristics of SRAM-based LUTs, namely non-negligible leakage current and volatility, studies on non-volatile memory based LUT have become promising. [1] proposes a novel LUT structure based on MRAM technology. The proposed LUT works only during a half-clock period of either high- or low-state, thereby reducing the static power at magnetic tunnel junction(MTJ). Since not only the structure but also the behavior of the LUT totally differs from existing SRAM based LUTs, a new CAD flow is required. This new CAD flow can place all cuts generated through the technology mapping process on the two types of LUTs—high or low state—so that the FPGA can work properly on time. However, commercial FPGAs have fixed configurations, which implies that the number of each type of LUTs are also fixed on the shelf. Thereby, we propose a novel technology mapping process ensuring a flexibility of placement of cuts with negligible performance degradation and increase in area. The flexibility can be calculated from the slack—the number of levels a cut can move. Figure 1 is an example of increasing slacks without changing the critical path or increasing the area. The simulation results—shown in table 1—shows the number of total slacks of each benchmark which are increased by 9.22% on average, while the delay and the area of each benchmark remains almost unaffected. We expect that this result will guarantee not only the flexibility of placement and routing steps but also better results by the end of the whole CAD flow.

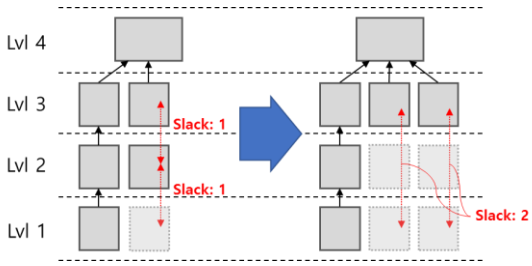

Fig 1. Increase in slack through proposed technology mapping

Benchmark		Delay	Total Slack	Area (# of LUTs)	Improvement (#/%)	
					Slack	Area
paj_framebuftop_hierarchy_no_mem	Conventional	8	4786	1037	240	-4
	Proposed	**8**	**5026**	**1033**	**5.01%**	**-0.39%**
binops	Conventional	2	66	70	6	0
	Proposed	**2**	**72**	**70**	**9.09%**	**0.00%**
oc54_cpu	Conventional	20	14380	2315	1785	95
	Proposed	**20**	**16165**	**2410**	**12.41%**	**4.10%**
diffeq_f_systemC	Conventional	15	2043	436	229	12
	Proposed	**15**	**2272**	**448**	**11.21%**	**2.75%**
cf_cordic_v_8_8_8	Conventional	4	1001	778	176	43
	Proposed	**4**	**1177**	**821**	**17.58%**	**5.53%**
bm_match3_str_arch	Conventional	7	615	136	0	0
	Proposed	**7**	**615**	**136**	**0.00%**	**0.00%**
					9.22%	**2.00%**

Table 1. Result of technology mapping applied

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[1] Kangwook Jo, Kyungseon Cho, and Hongil Yoon. "Variation-Tolerant and Low Power Look-Up Table(LUT) Using Spin-TORQUE Transfer Magnetic RAM for Non-volatile Field Programmable Gate Array(FPGA). 13th International SoC Design Conference (2016)